

**Notice of References Cited**Application No.  
09/421,437Applicant(s)  
David C. CHAPMANExaminer  
A.M. ThompsonGroup Art Unit  
2768

Page 1 of 2

**U.S. PATENT DOCUMENTS**

	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
A	5,303,161	4/1994	Burns et al.	364	490
B	5,856,927	1/1999	Greidinger et al.	364	491
C	6,014,507	1/2000	Fujii	395	500.13
D	6,011,912	1/2000	Yui et al.	395	500.14
E	5,483,461	1/1996	Lee et al.	364	490
F					
G					
H					
I					
J					
K					
L					
M					

**FOREIGN PATENT DOCUMENTS**

	DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS
N						
O						
P						
Q						
R						
S						
T						

**NON-PATENT DOCUMENTS**

	DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
U	Shirota et al., A New Rip-up and ReRoute Algorithm for Very Large Scale Arrays, IEEE Custom Integrated Circuits Conference, pp. 171-174	5/1996
V	M.H. Arnold et al., An Interactive Maze Router With Hints, Proceedings ACM/IEEE Design Automation Conference, pp. 672-676	6/1988
W	Pin-San Tzeng et al., Codar: A Congestion-Directed General Area Router, IEEE International Conference on Computer-Aided Design, pp. 30-33.	11/1988
X	L. -O Donzelle et al., A New Approach to Layout of Custom Analog Cells, Proceedings European Conference on Design Automation, pp. 480-483	2/1991

**Notice of References Cited**Application No.  
09/421,437Applicant(s)  
David C. CHAPMANExaminer  
A.M. ThompsonGroup Art Unit  
2768

Page 2 of 2

**U.S. PATENT DOCUMENTS**

	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
A					
B					
C					
D					
E					
F					
G					
H					
I					
J					
K					
L					
M					

**FOREIGN PATENT DOCUMENTS**

	DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS
N						
O						
P						
Q						
R						
S						
T						

**NON-PATENT DOCUMENTS**

	DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
U	E. Malavasi et al., Area Routing for Analog Layout, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, pp. 1186-1197	8/1993
V		
W		
X		